SC1600用户手册

2.4G低功耗射频收发芯片

Version 1.6

目录

1 缩略语

资料中用到的缩写词如下：

AGC	Automatic Gain Control	自动增益调节
ADC	Analog to Digital Converter	模/数转换器
APLL	Analog Phase Locked Loop	模拟锁相环
BPF	Band Pass Filter	带通滤波器
CRC	Cyclic Redundancy Check	循环冗余检查
DAC	Digital to Analog Converter	数/模转换器
ETSI	European Telecommunications Standards Institute	欧洲电信标准学会
FCC	Federal Communications Commission	（美国）联邦通信委员会
FEC	Forward Error Correction	前向误差校正
FIFO	First-In-First-Out	先进先出
GFSK	Gaussian Frequency Shift Keying	高斯移频键控
I/O	Input/Output	输入/输出
MCU	Microcontroller Unit	微控制器单元
MISO	Master In Slave Out	主入从出
MOSI	Master Out Slave In	主出从入
LDO	low dropout regulator	低压差线性稳压器
LNA	Low Noise Amplifier	低噪声放大器
LSB	Least Significant Bit/Byte	最低有效位/字节
PA	Power Amplifier	功率放大器
RF	Radio Frequency	射频
RSSI	Received Signal Strength Indicator	接收信号强度指示器
RX	Receive，Receive Mode	接收，接收模式
SPI	Serial Peripheral Interface	串行外设接口
TX	Transmit，Transmit Mode	发送，发送模式
VCO	Voltage Controlled Oscillator	电压控制振荡器
XTAL	Crystal	石英晶体

2 芯片简介

SC1600是一款低成本，高集成度的2.4GHZ的无线收发芯片，片上集成发射机、接收机、频率综合器和GFSK调制解调器。SC1600具有高灵敏度、低功耗以及抗干扰能力强的优点， 可适用于无线遥控、无线键鼠、无线通讯以及工业控制等领域。

SC1600片上的发射接收FIFO寄存器可以和MCU进行通信，存储数据，然后以1Mbps数据 率在空中传输。它内置了CRC、FEC、AUTO-ACK和重传机制，可以大大简化系统设计并优 化性能。同时外围电路简单，只需搭配MCU以及少数外围被动元件。为了提高电池使用寿命，

芯片在各个环节都降低功耗，芯片最低工作电压可以到1.9V，最低睡眠模式电流小于1μA。数字基带支持SPI和I2C接口，PKT_FLAG数字接口可作为MCU的中断输入。

3 芯片主要特点

低功耗的2.4GHz ISM频段、GFSK射频收发器 内嵌
8bit成帧器的64字节缓存区，可减轻MCU工作量 简单
的微处理器接口-SPI，I2C 强大的C/I提供良好的WIFI
共存性能 可编程数据白化和自动应答功能 支持
FEC，增加通信可靠性
支持16位CRC 支持AGC 高效的功耗管理模块
（最低约lμA待机电流）
外接晶振容许50PPM的变化
符合FCC/ETSI
110度工作温度，适用于LED灯（要求晶振的ppm在±50ppm以内）
近距离模式，适用于有特定安全需求的环境
可外接PA，增加通讯距离 支持
QFN20，SOP16，SOP8的封装

4 模块方框图

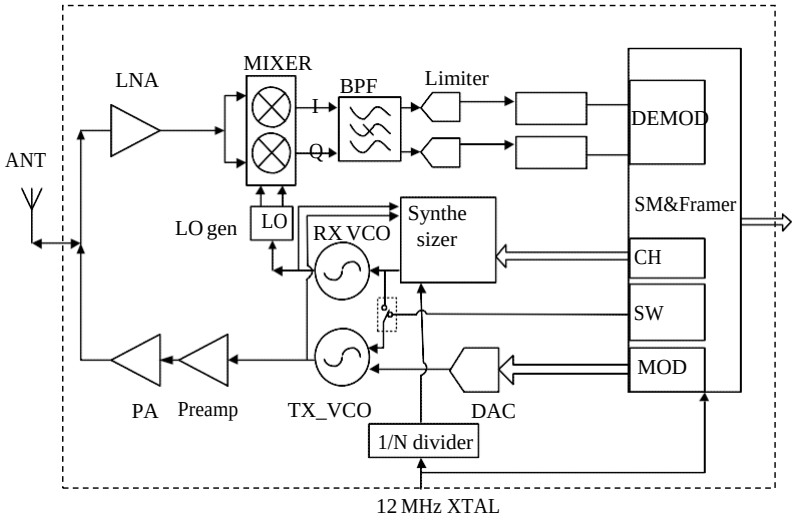


图**1 SC1600**模块方框图

5 电气特性

表**1**：电气特性（以下电气特性都是在工作温度**25℃**，工作电压**3.3V**条件下得到的）

参数	描述	规格			单位	说明
		最小	典型	最大		
T_{OP}	工作温度	-40		85	℃	1600H最高工作温度110℃
V_{DD}	工作电压	1.9		3.6	V	
F_xtal	晶体频率		12		MHz	50PPM tolerance
I_{DD_TX}	TX工作电流		18.5		mA	P_{OUT} = 0 dBm
I_{DD_RX}	RX 工作电流		16.5		mA	
I_{DD_IDLE}	IDLE工作电流		0.7		mA	
I_{DD_SLP}	Sleep 工作电流		2		μA	3.0V at ROOM temperature
F_{CLK}	输出时钟		12		MHz	
T_{r_spi}	SPI时钟沿上升下降的时间			25	ns	Requirement for error-free register reading, writing.
$F_{\_SPI}$	SPI时钟速度	0		12	MHz	
$F_{\_OP}$	工作频率	2402		2480	MHz	
VSWR	天线端口差异 (Z_0=50Ω)		<2:1		VSWR	
RXS	接收灵敏度		-87	-80	dBm	BER <= 0.1%
RXM	最大输入功率	-10			dBm	BER <= 0.1%
IIP_3	三阶输入截止点		-40		dBm	BER <= 0.1%
$R_{\_data}$	数据率		1E6		Bit/s	
$CI_{\_co\text{-}channel}$	同频干扰		9		dB	
$CI_{\_1MHz}$	1MHZ同频信号干扰		3		dB	-60 dBm desired signal.
$CI_{\_2MHz}$	2MHZ同频信号干扰		-15		dB	-60 dBm desired signal.
$CI_{\_3MHz}$	3MHZ同频信号干扰		-24		dB	-60 dBm desired signal.
$CI_{\_Image}$	Carrier/Interference at image frequency		-10		dB	-67 dBm desired signal.
$CI_{\_3MHzUp}$	Carrier/Interference at>3MHz offset		-27		dB	-60 dBm desired signal.
OBB_1	带外干扰	-30			dBm	30 MHz to 2000 MHz
OBB_2			-10		dBm	2000 MHz to 2400 MHz

参数	描述	规格			单位	说明
		最小	典型	最大		
OBB_3			-10		dBm	3000 MHz to 12.75 GHz
P_{out_max}	最大发射功率		3		dBm	
$DF1_{avg}$	最大频偏 00001111 pattern		350		kHz	Modulation Characteristics TX EYE diagram
$DF2_{max}$	最大频偏 01010101 pattern		300		kHz	Modulation Characteristics TX EYE diagram
$DF2_{max}$ / $DF1_{avg}$	TX EYE opening	80			%	1010 data sequence referenced to 00001111 data sequence
IBS_1	带内辐射(+/550kHz)			-20	dBm	Random data
IBS_2	带内辐射2MHz偏移			-40	dBm	Random data
IBS_3	带内辐射3MHz 偏移			-60	dBm	Random data
OBS_1	带外辐射			-60	dBm	30 MHz ~ 1 GHz
OBS_2				-45	dBm	1 GHz ~ 12.75 GHz
OBS_3				-60	dBm	1.8 GHz ~ 1.9 GHz
OBS_4				-65	dBm	5.15Hz ~ 5.3 GHz

6 管脚描述

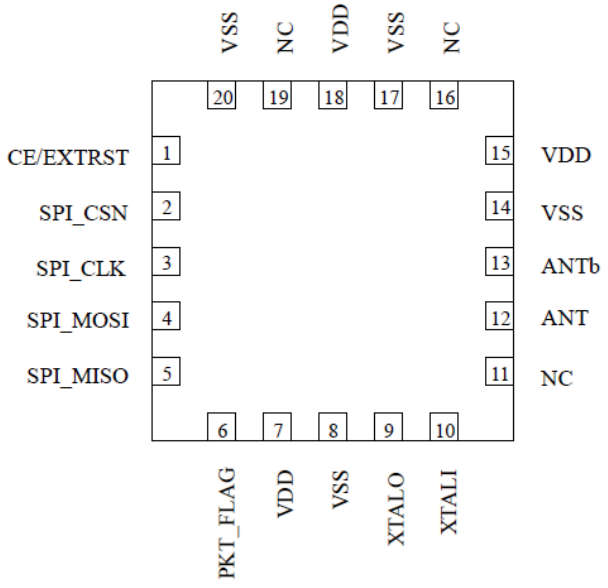


图**2 SC1600 QFN20**封装示意图

表**2**：**QFN20**管脚描述

管脚编号	管脚名	管脚类型	描述
1	CE/EXTREST	数字输入	芯片使能、复位信号，1-芯片使能，0-芯片复位
2	SPI_CSN	数字输入	SPI接口片选信号
3	SPI_CLK	数字输入	SPI时钟，I2C 时钟（ *默认***SPI**接口）
4	SPI_MOSI	数字输入	SPI Slave Data Input，I2C A5
5	SPI_MISO	数字输出	SPI Slave Data Output,I2C Data***(****默认***SPI**接口***)***
6	PKT_FLAG	数字输出	发送、接收包完成标志位
7	VDD	电源	输入电压
8	VSS	地	地
9	XTALO	模拟输出	晶体振荡器输出脚
10	XTALI	模拟输入	晶体振荡器输入脚
11	NC		无连接
12	ANT	射频端口	天线接口
13	ANTb	射频端口	天线接口
14	VSS	地	地
15	VDD	电源	输入电压
16	NC		无连接
17	VSS	地	地
18	VDD	电源	输入电压
19	NC		无连接
20	VSS	地	地

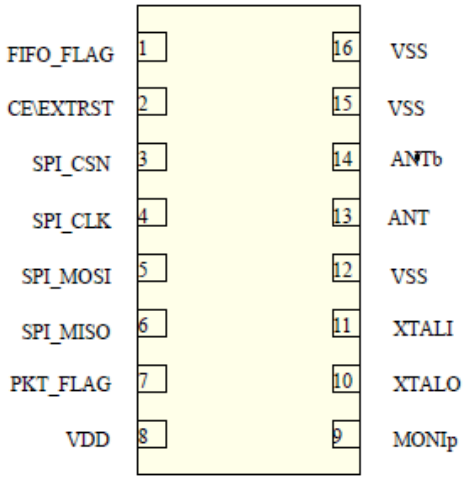


图**3 SC1600 SOP16**封装示意图

表**3 SOP16**管脚描述

管脚编号	管脚名	管脚类型	描述
1	FIFO_FLAG	数字输出	FIFO空或满标志位
2	CE/EXTREST	数字输入	芯片使能、复位信号，1-芯片使能，0-芯片复位
3	SPI_CSN	数字输入	SPI接口片选信号
4	SPI_CLK	数字输入	SPI时钟，I2C 时钟（*默认***SPI**接口）
5	SPI_MOSI	数字输入	SPI Slave Data Input，I2C A5
6	SPI_MISO	数字输出	SPI Slave Data Output，I2C Data（*默认***SPI**接口）
7	PKT_FLAG	数字输出	发送、接收包完成标志位
8	VDD	电源	输入电压
9	MONIp	模拟输出	测试专用脚
10	XTALO	模拟输出	晶体振荡器输出脚
11	XTALI	模拟输入	晶体振荡器输入脚
12	VSS	地	地
13	ANT	射频端口	天线接口
14	ANTb	射频端口	天线接口
15	VSS	地	地
16	VSS	地	地

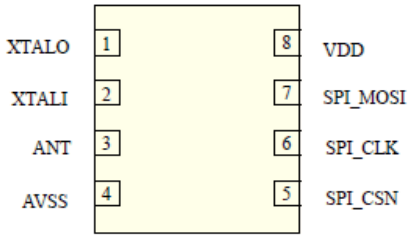


图**4 SC1600 SOP8**封装示意图

表**4 SOP8**管脚描述

管脚编号	管脚名	管脚类型	描述
1	XTALO	模拟输出	晶体振荡器输出脚
2	XTALI	模拟输入	晶体振荡器输入脚
3	ANT	射频端口	天线接口
4	AVSS	地	地
5	SPI_CSN	数字输入	SPI接口片选信号
6	SPI_CLK	数字输入	SPI时钟
7	SPI_MOSI	数字IO	SPI Slave Data Input/Output
8	VDD	电源	输入电压

7 典型应用

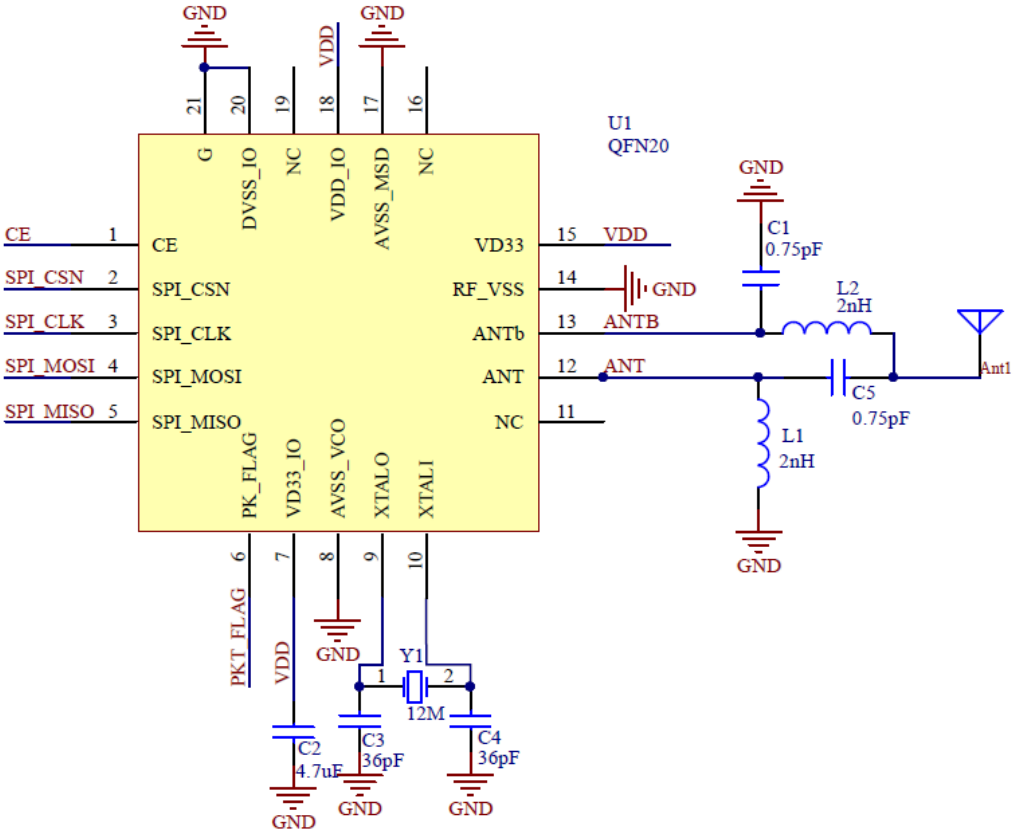


图5 **SC1600 QFN20**典型应用图

表5 **SC1600 QFN20**典型应用元件清单

数量	原理图标识	值	封装	描述
2	C1,C5	0.75pF	0603	murata, ±0.2PF, 50V
1	C2	4.7μF	0603	murata, ±5%, 50V
2	C3,C4	36pF	0603	murata, ±5%PF, 50V
2	L1,L2	2nH	0603	murata, ±0.2nH
1	Y1	12M	3225	<±50ppm ESR<60Ω
1	U1	SC1600	QFN20	

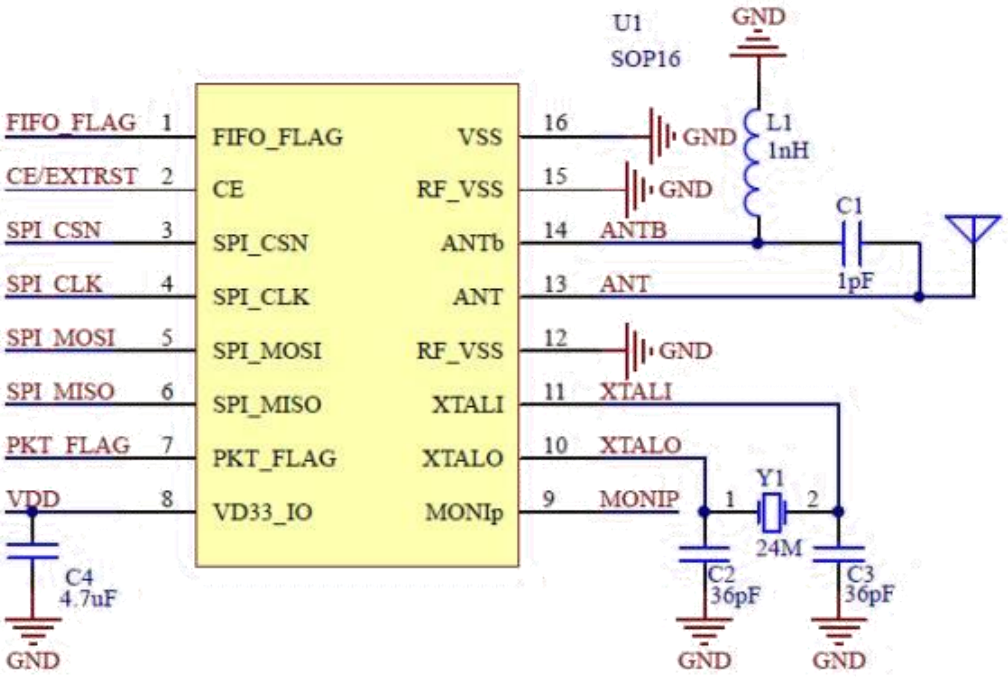


图6 SC1600 SOP16典型应用图

表**6 SC1600 SOP16**典型应用元件清单

数量	原理图标识	值	封装	描述
1	C1	1pF	0603	murata, ±0.2PF, 50V
2	C2,C3	36pF	0603	murata, ±5%PF, 50V
1	C4	4.7μF	0603	murata, ±5%, 50V
1	L2	1nH	0603	murata, ±0.2nH
1	Y1	12M	3225	<±50ppm ESR<60Ω
1	U1	SC1600	SOP16	

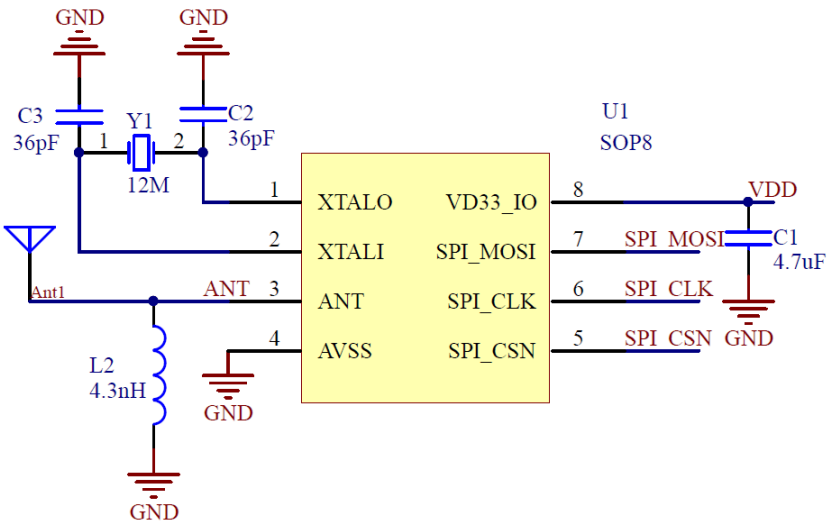


图7 **SC1600 SOP8**典型应用图

表7 SC1600 SOP8典型应用元件清单

数量	原理图标识	值	封装	描述
1	C1	4.7μF	0603	murata, ±5%PF,50V
2	C2,C3	36pF	0603	murata, ±5%PF,50V
1	L2	4.3nH	0603	murata, ±0.2nH
1	Y1	12M	3225	<±50ppm ESR<60Ω
1	U1	SC1600	SOP8	

*天线的L和C，需要根据实际PCB设计调整到最佳值；

*晶体的C，需要根据不同晶体调整到最佳值。

8 SPI INTERFACE

8.1 SPI SEQUENCE

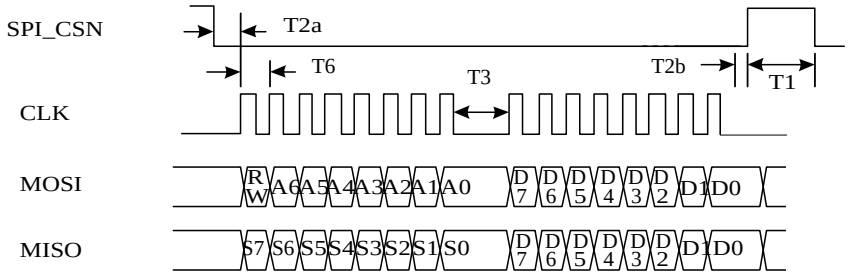


Figure 8-1 4wire SPI R/W Register sequence（CKPHA=1）

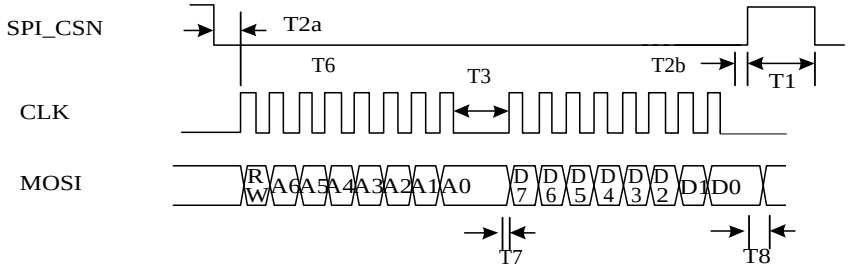


Figure 8-2 3wire SPI Read Register sequence（CKPHA=1）

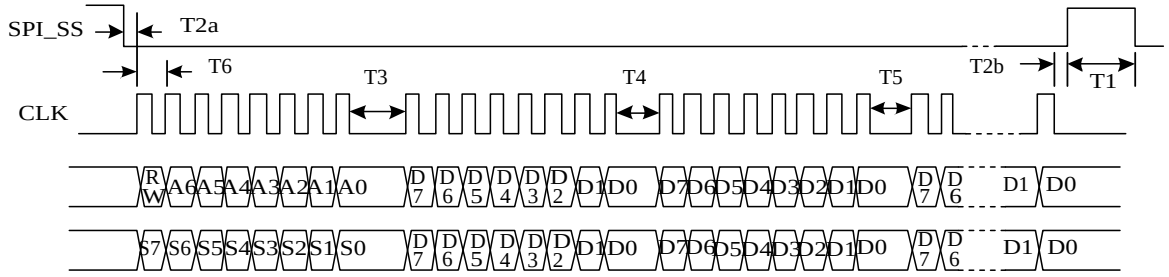


Figure 8-3 SPI R/W FIFO sequence（CKPHA=1）

Notice：

1)SPI R/W bit: writing=0,read=1;

2)When access FIFO , you can r/w FIFO continuously only write address once;

3)When access registers except FIFO, you can only access one byte during one CS duty.

Table 8 SPI timing request

参数	描述	规格			单位	说明
		MIN	TYP	MAX		

参数	描述	规格			单位	说明
		MIN	TYP	MAX		
T1	Minimum SPI inactive time	250			ns	
T2a	Setup time of SS	20			ns	
T2b	hold time of CSN	200			ns	
T3，T4，T5		450			ns	When access to FIFO
T6		83			ns	
T7	Time from rising edge of SPI clock to SC1600 data output	0		10	ns	
T8	Time from rising edge of SPI CSN to MOSI change to SC1600 data input			220	ns	

9 I2C INTERFACE

(SOP8 package is not available, you can contact to us for customization)

9.1 I2C FEATURE

Speed: 100kbit/s ~ 400kbit/s;

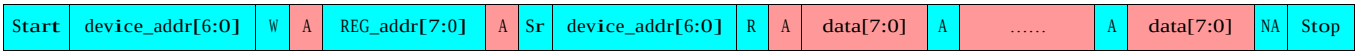
Address: Device Address is 7bit;

Device Address:0xx1000b（the value of bit 4 equals to bit7 of address@30,and the value of bit 5 equals to PIN SPI_MOSI level）.

9.2 I2C SEQUENCE

Write data to specified register address

Read data from specified register address



Read FIFO without adress specification

(注：表示master；表示slave)

10 RECEPTION/TRANSMITION FLOWS

10.1 Init RF

① : set PIN CE to high level to enable chip(if chip have PIN CE);

② : choose SPI or IIC mode(address@30) and 3-wire/4-wire SPI mode(address@94);

③ : you should write following data into related registers to init chip.

Address@1=0xE9, Address@2=0x57, Address@3=0x0D, Address@4=0xC4

Address@8=0x25, Address@9=0x14, Address@10=0x45, Address@11=0x1B

Address@16=0x84, Address@17=0x5A, Address@18=0x08, Address@19=0x00

Address@27=0xA4, Address@33=0x03, Address@34=0x13, Address@35=0xC0

Address@46=0x01, Address@47=0x15, Address@49=0x5B, Address@50=0x15,

Address@51=0x14, Address@52=0x00, Address@53=0x00, Address@64=0x78

Address@72=0x61, Address@73=0x07, Address@74=0x17, Address@75=0x94

Address@76=0xED, Address@77=0x27, Address@78=0x75, Address@79=0x66

④ : choose package encoding type(address@65),FEC type(address@65)(transmit device should be the same to reception device);

⑤ : set up the frame(address@64,@81),syncword(address@72,@73,@74,@75,@76,@77,@78,@79) (transmit device should be the same to reception device);

10.2 Transmit flow "small packet"(<=64bytes)

After Init RF(details at 10.1 part),the transmit flow should add following steps:

① : setup transmit power gain(address@18);

② : setup transmit frequency channel(address@15);

③ : clean TX FIFO(address@104);

④ : write data length into FIFO(address@100);

⑤ : write data into FIFO(address@100), and the data length should not bigger than length;

⑥ : write address@52=0x1A,clear address@15.bit7,set address@14.bit0,and the data in

FIFO will be sent ,and you will get a transmit complete flag on PIN PKT=HIGH or pkt_flag(address@97)=1(and now RF is in IDLE mode);

⑦ : then you can transmit other data by repeat step ③④⑤ or turn to reception flow(Part 10.3).

10.3 Reception flow "small packet"(<=64bytes)

After Init RF(details at 10.1 part),the reception flow should add following steps:

① : choose short distance mode or normal working mode;

② : set up reception frequency channel(address@15);

③ : clean RX FIFO(address@105);

④ : write address@52=0x1E, clear address@14.bit0, set address@15.bit7,wait for PKT PIN=HIGH level or pkt_flag=1(address@97)(this means that a packet has been received),then clear pkt_flag(addresss@33),

⑤ : check the CRC_error flag(address@96),if CRC_error flag=0, you can get the data from FIFO(address@100), and the first byte you get is the length that you need to read next ;if CRC_error flag=1, you should repeat step ③④ to wait for another package.

⑥ : then you can repeat step ③④⑤ to receive new data or turn to transmit flow(Part 10.2).

10.4 Transmit flow "large packet"(<255bytes and >64bytes)

After Init RF(details at 10.1 part),the transmit flow(large packet) should add following steps :

① : write address@33=0;

② : setup transmit power gain(address@18) , then write address@33=0x03;

③ : setup transmit frequency channel(address@15);

④ : clean TX FIFO(address@104);

⑤ : write data length into FIFO(address@100);

⑥ : write data into FIFO(address@100)(because the FIFO space is 64 bytes, so you can write 63 bytes here), write address@52=0x1A,clear address@15.bit7,set address@14.bit0;

⑦ : check the FIFO flag(address@97) and PKT flag(address@97), if FIFO flag=1 but PKT flag=0, you can write new data into FIFO(the data length should not bigger than 64-

FIFO_FULL_THRESHOLD(address@80,@81));

⑧ : you can repeat step ⑦ until PKT flag=1(PIN PKT=HIGH pkt_flag(address@97)=1); this means that the large packet has been transmitted completely;

⑨ : then you can transmit other data by repeat step ③-⑧ or turn to reception flow.

10.5 Reception flow "large packet"(<255bytes and >64bytes)

① : write address@33=0x03;

② : clean RX FIFO(address@105);

③ : setup transmit frequency channel(address@15); write address@52=0x1E, clear address@14.bit0, set address@15.bit7;

④ : check the FIFO flag(address@97) and PKT Flag, if FIFO flag=1, now you should get data from FIFO(address@100), and if in bad environment, MCU should have a timer to avoid waiting for FIFO flag;

⑤ : if PKT flag=1(address@97),this means this big packet has successfully received;

⑥ : then you can receive other data by repeat step ③-⑤ or turn to transmit flow.

10.6 Enter Idle Mode flow

To Enter Idle Mode flow should add following steps:

① : clear address@14.bit0, clear address@15.bit7;

10.7 Enter Sleep Mode flow

After Init RF(details at 10.1 part),To enter Sleep mode flow should add following steps:

① : set SLEEP_ENABLE bit(address@70)

10.8 Wake Up From Sleep Mode flow

When RF is in sleep mode, following steps can wake up RF and enter idle mode:

① : keeping PIN SPI_CSN in low level for 1ms-2ms.

10.9 Scan RSSI flow

After Init RF(details at 10.1 part), following steps are the scan RSSI flow:

① : open RSSI function(address@22), the lowest two bits should be 0;

② : set the number of channels need to scan;

③ : set the first scan channel(also named RSSI offset channel);

④ : start scan RSSI(address@86);

⑤ : wait the PKT flag=1(address@97), then you can get the RSSI value of channels from FIFO(address@100).

11 REGISTER DISCRIPTION

You can access following registers by I2C or SPI, other registers are only for testing, please do not modify them.

Address@14 Default value:0x00 R/W

Bit	Bit Name	Description
7-1	reserve	
0	Start_TXFIFO	Write 1 to start transmitting the data in FIFO, after transmit completely, this bit will auto cleared by hardware, you should rewrite this bit to 1 to enter reception mode if needed.

Address@15 Default value:0x30 R/W

Bit	Bit Name	Description
7	Start_RX	Write 1 to enter reception mode, after receive a valid packet, this bit will auto cleared by hardware, you should rewrite this bit to 1 to enter reception mode if needed.
6-0	Frequency_Channel	The frequency channel= 2402+ Frequency Channel (MHz).

Address@18 Default value:0x79 R/W

Bit	Bit Name	Description
7-4	TX_PA	Transmit power gain.
3-0	reserve	

Address@22 Default value:0x03 R/W

Bit	Bit Name	Description
7-2	reserve	
1-0	RSSI_DISABLE	=11,disable RSSI function; =00,enable RSSI function.

Address@30 Default value:0x80 R/W

Bit	Bit Name	Description
7	SPI_CPHA	=1,data capture on the second clock edge; =0,data capture on the first clock edge; (In I2C mode equal to 0xA4-MISO PIN In I2C mode equal to 0xA5-MOSI PIN)
6	I2C_MODE	=1,I2C mode enable and spi mode disable; =0,I2C mode disable and spi mode enable;
5-0	reserve	

Address@37 Default value:0x00 R/W

Bit	Bit Name	Description
7-2	reserve	
1	CLEAR_PKT_FLAG	Write 1 to clear pkt_flag.
0	CLEAR_FIFO_FLAG	Write 1 to clear FIFO flag.

Address@64 Default value:0x18 R/W

Bit	Bit Name	Description
7-5	PREAMBLE_LEN	Preamble length=1+ PREAMBLE_LEN.(byte)

4-3	SYNCWORD_LEN	=11:syncwordtength is 8 bytes {contents are @Address79+ @Address78+ @Address77 +@Address76+ @Address75+ @Address74+ @Address73+ @Address72}; =10:syncwordtength is 6 bytes { contents are @Address79+ @Address78+ @Address77 +@Address76+ @Address73+ @Address72} =01:syncwordtength is 4 bytes { contents are @Address79+ @Address78+ @Address73+ @Address72} =00:syncwordtength is 2 bytes { contents are @Address73+ @Address72} Notice: more details refer to @Address 81
2-0	TRAILER_LEN	trailer length=4+(2* TRAILER_LEN)(bits)

Address@65 Default value:0x00 R/W

Bit	Bit Name	Description
7-6	PACKET_ENCODING_TYPE	=00:encoding type is NRZ law data type =01:encoding type is Manchester data type =10:encoding typeis 8/10 line code =11:encoding type is interleave date type
5-4	FEC_TYPE	=00:No FEC =01:FEC13 =10:FEC23
3-0	reserve	

Address@70 Default value:0x03 R/W

Bit	Bit Name	Description
7	reserve	

6	SLEEP_ENABLE	Write 1 to enter sleep mode
5	LNA_Off_Mode	=1:short distance mode =0:normal working mode
4-0	reserve	

Address@80 Default value:0x20 R/W

Bit	Bit Name	Description
7-3	FIFO_EMPTY_THLD	FIFO empty threshold
2-0	FIFO_FULL_THLD_H	FIFO full threshold high bits

Address@81 Default value:0x47 R/W

Bit	Bit Name	Description
7-6	FIFO_FULL_THLD_L	FIFO full threshold low bits
5-0	SYNCWORD_THRESHOLD	The value of SYNCWORD_THRESHOLD must equal to (syncword tength-1)

Address@84 Default value:0xFD R/W

Bit	Bit Name	Description
7-2	SCAN_RSSI_CH_NUM	The number of channels for scanning RSSI, and the RSSI value will be store into FIFO
1-0	reserve	

Address@86 Default value:0x00 R/W

Bit	Bit Name	Description
7	START_SCAN_RSSI	Write 1 to start scan RSSI, this bit will be cleared by hardware if scan completely.
6-0	CHANNEL_OFFSET_OF_RSSI_SCAN	Scan RSSI from (2402+ CHANNEL_OFFSET_OF_RSSI_SCAN)MHz channel

Address@87 Default value:0x0F R/W

Bit	Bit Name	Description
7	reserve	
6-0	RSSI_STABLE_TIME	When RSSI scanning, set the VCO and SYN stable time,1us per step.

Address@94 Default value:0x00 R/W

Bit	Bit Name	Description
7	THREE_WIRE_SPI_EN	=1,switch to 3-wire SPI interface =0,switch to 4-wire SPI interface
6-0	reserve	

Address@96 Default value:0x60 RO

Bit	Bit Name	Description
7	CRC_VERIFY_FLAG	=1,CRC verify error; =0,CRC verify ok.
6-0	reserve	

Address@97 Default value:0x61 RO

Bit	Bit Name	Description
7	reserve	
6	PKT_FLAG	Receive/transmit packet completely flag
5	FIFO_FLAG	FIFO empty/full flag
4-0	reserve	

Address@100 Default value:0x00 R/W

Bit	Bit Name	Description
7-0	FIFO_DATA	The data to need to be transmitted or data had been received.

Address@104 Default value:0x00 R/W

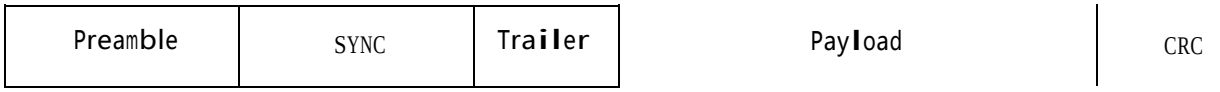
Bit	Bit Name	Description
7	CLR_ W_PTR	Write 1 to clear the write FIFO point;

		When reading, it always return 0.
6	reserve	
5-0	FIFO_W_PTR	FIFO write pointer, read only.

Address@105 Default value:0x00 R/W

Bit	Bit Name	Description
7	CLR_ R_ PTR	Write 1 to clear the read FIFO point; When reading, it always return 0.
6	reserve	
5-0	FIFO_R_PTR	FIFO read pointer, read only.

12 Packet Frame



Preamble:1 ~ 8bytes,programmable.

SYNC:16/32/48/64bits,programmable as device SYNCWORD.

Trailer:4 ~ 18bits,programmable.

Payload: TX/RX data.

CRC:16-bit CRC is optional.

13 电源要求

避免使用变频DC-DC变换，特别是变换频率在50kHz以下直流变换器会干扰RF通讯，电机系统内不要省电容（滤波电容）；2μA的sleep电流指的是常温下的情况，高温下sleep电流会上升到>20μA，这是由MOS的漏电特性决定，非电路设计问题。

14 发射功率的调整

表9 发射功率的调整

Register1	TXP

8的值 (Hex)	SOP16	SOP8	unit
08	3.2	1.0	dBm
18	2.5	0.3	dBm
28	1.6	-0.6	dBm
38	0.7	-1.4	dBm
48	0.0	-2.2	dBm
58	-1.0	-3.0	dBm
68	-2.0	-4.0	dBm
78	-3.3	-5.3	dBm
88	-4.8	-6.8	dBm
98	-5.7	-7.7	dBm
A8	-6.8	-8.8	dBm
B8	-8.1	-10.0	dBm
C8	-9.5	-11.6	dBm
D8	-11.3	-13.3	dBm
E8	-13.6	-15.6	dBm
F8	-16.6	-18.7	dBm

15 天线及匹配

匹配的第一要求是50ohm阻抗线，第二准则是长线串电容谐振消除，宽线并电感谐振消除。如果不按照手册中推荐的封装，而是定制封装，由此造成不同的天线管脚位置，那么匹配需 要根据实际进行相应的调整。

比如封装采用的方案只留出一个ANT管脚且该管脚置于SOP16的第16脚，由于Bonding线较长，建议这种情况下匹配改为下图所示：

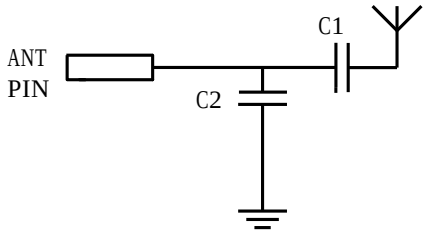
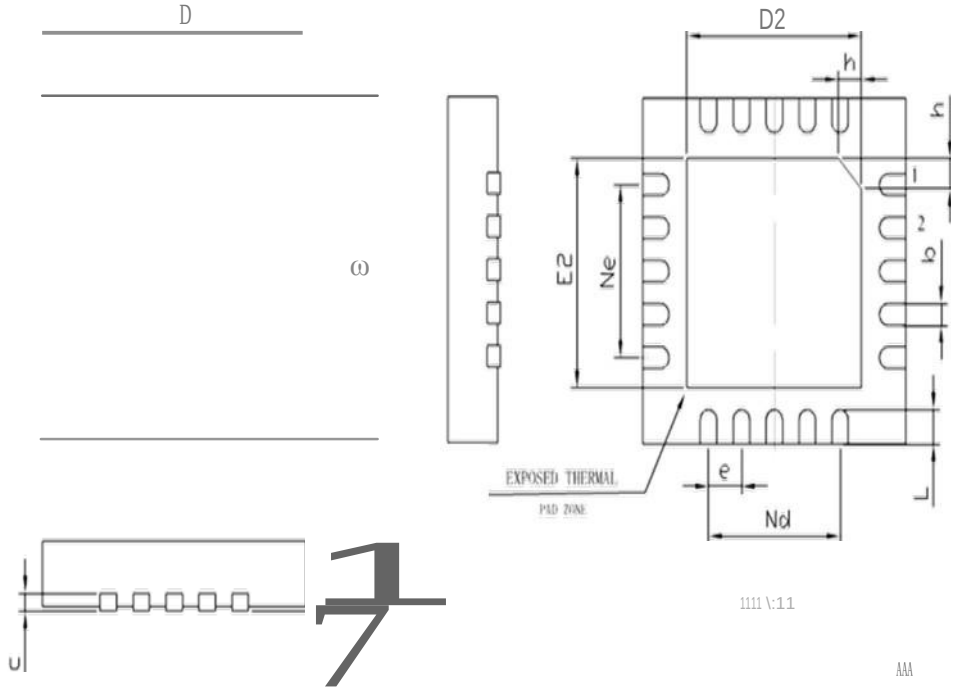


表10 原件清单

原理图标识	值	封装	描述
C1	3pF	0603	murata, ±0.2pF,50V
C2	1pF	0603	murata, ±0.2pF,50V

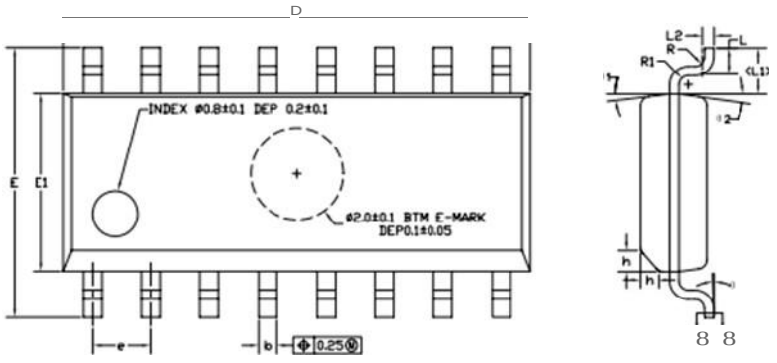
16

QFN20



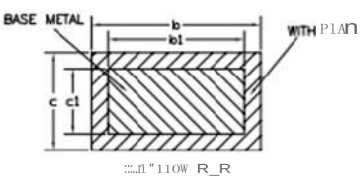
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1		0.02	0.05
b	0.15	0.20	0.25
c		REF	
c1		0.203 REF	
D		4.00 BSC	
D2	2.60	2.70	2.80
e		0.50 BSC	
E		4.00 BSC	
E2	2.60	2.70	2.80
L	0.35	0.40	0.45
h	0.30	0.35	0.40

SOP16



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.55	0.65	0.75
b1	0.36		0.51
c	0.35	0.40	0.45
c1	0.17	-	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27BSC	
L	0.45	0.60	.80
L1		1.04REF	
L2		0.25BSC	
R	0.07		-
R1	.07	-	
h	0.30	0.40	0.50
θ	0		8
θ1	6	If	15
θ2	6	11	13
θ3	5	11	13
θ4	5	11	13



NOTES:
ALL DIMENSIONS MEET JEDEC STANDARD MS-012 AC
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS

SOP8